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AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A nonvolatile semiconductor storage unit comprising:

a plurality of word lines;

~~a plurality of bit lines;~~

a plurality of memory cells connected to a bit line, each memory cell being ~~of which is correspondingly~~ connected to a corresponding one of said word lines ~~and one bit line~~ and ~~has~~ having a control gate and a floating gate;

a sense latch circuit having a first node and a second node, wherein said first node ~~which~~ is connected to one end of said bit line, ~~and detects~~ said sense latch circuit detecting data on said bit line ~~correspondingly~~ corresponding to a threshold voltage ~~for said~~ of a selected memory cell;

a MOSFET ~~which is~~ connected between said bit line and said sense latch circuit, ~~uses~~ said MOSFET having ~~its~~ a gate coupled to receive said data on said bit line, and ~~drives a~~ said MOSFET driving said second node ~~for~~ of said sense latch circuit;

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a bit line precharge circuit which is connected to said bit line and which precharges said bit line; and

a power supply circuit which is connected to said bit line precharge circuit and which generates precharge voltage for said bit line ~~dependently on~~ according to a threshold voltage of said MOSFET.

2. (currently amended) The nonvolatile semiconductor storage unit according to claim 1,

wherein said bit line precharge circuit can supply first and second ~~potentials with different~~ voltages having voltage levels different from each other ~~values~~ and can further ~~comprises a~~ function to discharge said bit line,

wherein said bit line precharge circuit is supplied with said first ~~potential~~ voltage when precharging said bit line, and

wherein said bit line precharge circuit is supplied with said second ~~potential~~ voltage when discharging said bit line.

3. (currently amended) The nonvolatile semiconductor storage unit according to claim 2, further comprising:

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a bit line selective precharge circuit which is connected to said bit line and which selectively precharges said bit line,

wherein said bit line selective precharge circuit can supply third and fourth ~~potentials with different~~ voltages having different voltage levels from each other ~~values~~ and ~~further comprises a function to~~ determines data in said sense latch circuit in cooperation with said bit line precharge circuit,

wherein, when selectively precharging said bit line, said bit line selective precharge circuit is supplied with said third ~~potential~~ voltage, and

wherein, when determining data in said sense latch circuit, said bit line selective precharge circuit is supplied with said fourth ~~potential~~ voltage and said bit line precharge circuit is supplied with said second ~~potential~~voltage.

4. (currently amended) The nonvolatile semiconductor storage unit according to claim 1, further comprising:

a selection circuit which is connected to ~~a~~ one of said first and second nodes of said sense latch circuit and ~~interchanges~~ which inputs/outputs data between said sense

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latch circuit and a common input/output line,

wherein said selection circuit can supply fifth and sixth ~~potentials with different~~ voltages having different voltage levels from each other ~~values~~ and ~~further comprises a function to~~ precharges and discharges ~~the~~ said one of said first and second nodes ~~for said sense latch circuit~~,

wherein said selection circuit makes connection between said sense latch circuit and said common input/output line when inputting/outputting data ~~is exchanged~~ therebetween,

wherein said selection circuit is supplied with said fifth ~~potential~~ voltage when ~~the~~ said one of said first and second nodes ~~for said sense latch circuit~~ is precharged, and

wherein said selection circuit is supplied with said sixth ~~potential~~ voltage when ~~the~~ said one of said first and second nodes ~~for said sense latch circuit~~ is discharged.

5. (currently amended) The nonvolatile semiconductor storage unit according to claim 1,

wherein sources of said plurality of memory cells are commonly connected to a common line via a second MOSFET ~~whose source is~~ driven by a gate control signal, and

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wherein a gate of each memory cell is connected to ~~each~~ the corresponding word line and a drain thereof is commonly connected to ~~a~~ said bit line.

6. (previously presented) The nonvolatile semiconductor storage unit according to claim 1,

wherein each of said plurality of memory cells can store a plurality of bits of data as a threshold voltage.

7. (currently amended) The nonvolatile semiconductor storage unit according to claim 2,

wherein sources of said plurality of memory cells are commonly connected to a common line via a second MOSFET ~~whose source is~~ driven by a gate control signal, and

wherein a gate of each memory cell is connected to ~~each~~ the corresponding word line and a drain thereof is commonly connected to ~~a~~ said bit line.

8. (currently amended) The nonvolatile semiconductor storage unit according to claim 3,

wherein sources of said plurality of memory cells are commonly connected to a common line via a second MOSFET ~~whose source is~~ driven by a gate control signal, and

wherein a gate of each memory cell is connected to

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~~each~~ the corresponding word line and a drain thereof is commonly connected to ~~a~~ said bit line.

9. (currently amended) The nonvolatile semiconductor storage unit according to claim 4,

wherein sources of said plurality of memory cells are commonly connected to a common line via a second MOSFET ~~whose source is~~ driven by a gate control signal, and

wherein a gate of each memory cell is connected to ~~each~~ the corresponding word line and a drain thereof is commonly connected to ~~a~~ said bit line.

10. (previously presented) The nonvolatile semiconductor storage unit according to claim 2,

wherein each of said plurality of memory cells can store a plurality of bits of data as a threshold voltage.

11. (previously presented) The nonvolatile semiconductor storage unit according to claim 3,

wherein each of said plurality of memory cells can store a plurality of bits of data as a threshold voltage.

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12. (previously presented) The nonvolatile semiconductor storage unit according to claim 4,

wherein each of said plurality of memory cells can store a plurality of bits of data as a threshold voltage.

13. (new) A nonvolatile semiconductor storage unit, comprising:

a nonvolatile memory cell capable of storing data as a threshold voltage thereof;

a bit line coupled to said nonvolatile memory cell;

a first MOSFET having a gate terminal thereof coupled to said bit line, a first terminal and a second terminal;

a second MOSFET having a source-drain path coupled to said bit line;

a sense amplifier having a first node thereof coupled to said first terminal of said first MOSFET and a second node thereof coupled to said source-drain path of said second MOSFET, and sensing a voltage level of said bit line;

a precharge circuit to supply a precharge voltage to said bit line in response to reading data stored in said nonvolatile memory cell; and

a precharge control circuit to supply a control

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signal to said precharge circuit,

wherein said precharge control circuit is adapted to control said precharge control signal, which is used for supplying said precharge voltage to said bit line in accordance with variations of a threshold voltage of said first MOSFET when supplying said precharge voltage to said bit line before said sensing.

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